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SUMMARY

This final report on Contract F30602-78-C-0352 summarizes the work performed to design, fabricate, and test a Microwave Transversal Equalizer (MTE) operating in the 3.05 to 3.55 GHz frequency range. The objective was to determine and evaluate the transfer characteristics of various microwave components and devices and the capability of reducing time side-lobe distortion in a microwave/radar system. The transfer characteristics relate the amplitude and phase response, or corresponding time side-lobe response, to a measured distortion level. The MTE developed for this program has been designed to artificially generate a train of 16 leading and 16 lagging time side-lobe echoes (relative to the mainline response) with a 3.3-ns spacing such that each echo is separately adjusted, both in amplitude and phase, to reduce time side-lobe distortion. Measured data resulted in the MTE reducing an induced -8 dB side-lobe echo to approximately -35 dB and a -18 dB side-lobe echo to approximately -40 dB (relative to mainline signal level).

The insertion loss of the MTE is approximately 2 dB and the input/output VSWR is less than 1.2:1. Both stability and repeatability measurements resulted in achieving an MTE output variation of less than 0.25 dB.

The MTE was mounted in an RFI enclosure to minimize external interference and is capable of including additional control devices without extensive hardware modifications. An input power of 110 Vac, 60 Hz is required to operate the MTE.

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We wish to express our appreciation for the technical direction of W. Peterson and D. Mokry of RADC, Griffiss Air Force Base, Rome, N. Y.

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EVALUATION

This Final Technical Report covers research and development work on a Microwave Transversal Equalizer, performed under Contract F30602-78-C-0352, during the period 31 March 77 through January 80. The objective of the program was to design and fabricate a closed loop transversal equalizer that would equalize waveforms so a transmitter's distortive effects could be minimized. Techniques studied during the contract included methods of manually and digitally controlling the amount of equalization.

The contract resulted in a unique piece of equipment that allows the engineer to use time domain techniques to reduce matched filter sidelobes from a -17 db to -35 db in the 3.0 GHz to 3.5 GHz frequency range.

The exploratory development work accomplished under this contract supports the Air Force C³ mission by advancing the performance capability of wideband high power transmitters of present and future radar and communication systems.



WILLARD PETERSON
Project Engineer

1. INTRODUCTION

A Microwave Transversal Equalizer (MTE) is required for use in the RADC High Power Lab to determine and evaluate the transfer characteristics of a variety of microwave components and devices. The transfer characteristics relate the amplitude and phase response, or the corresponding time side-lobe response, to a measured distortion level. By placing the microwave device in a loop containing the MTE, the desired response can be rapidly obtained by adjusting the equalizer to cancel the noted distortion effects. The transfer characteristics may then be related to the final MTE adjustment settings with the use of suitable algorithms.

RF distortion effects are evidenced by signal phase and amplitude deviations in the frequency domain (over the operating RF bandwidth), or a corresponding spurious side-lobe echo pattern in the time domain (over the operating range window). Distortion effects are due to the nonideal phase and amplitude characteristics of the microwave components and/or devices located within the system.

Deviations from phase linearity and flat gain response in a band-limited pulsed signal system (as viewed in the frequency domain) manifest themselves as pairs of echoes in time domain analysis--one preceding, and one following the main signal lobe by the same interval in each pair as shown in Figure 1.

Side-lobe distortion is most conveniently interpreted with paired echo theory (reference 1). Gain and phase characteristics can be expressed in terms of distortionless (flat gain and linear phase) components plus Fourier or periodic components. The side-lobe levels are given in decibels by:

$$S_1 = 20 \log \frac{2}{\left(\frac{a_n}{a_o} \right)} \quad (1)$$

$$S_2 = 20 \log \frac{2}{|b_n|} \quad (2)$$

$$S_3 = 20 \log \frac{2}{\left(\left| \frac{a_n}{a_o} \right| + |b_n| \right)} \quad (3)$$

where:

S_1 = side-lobe level for amplitude distortion

S_2 = level for phase distortion

S_3 = worst or lowest level for phase and amplitude distortion
of the same periodicity

and

$\frac{a_n}{a_o}$, b_n are the peak voltage amplitude and phase distortion
respectively for the n 'th periodic component

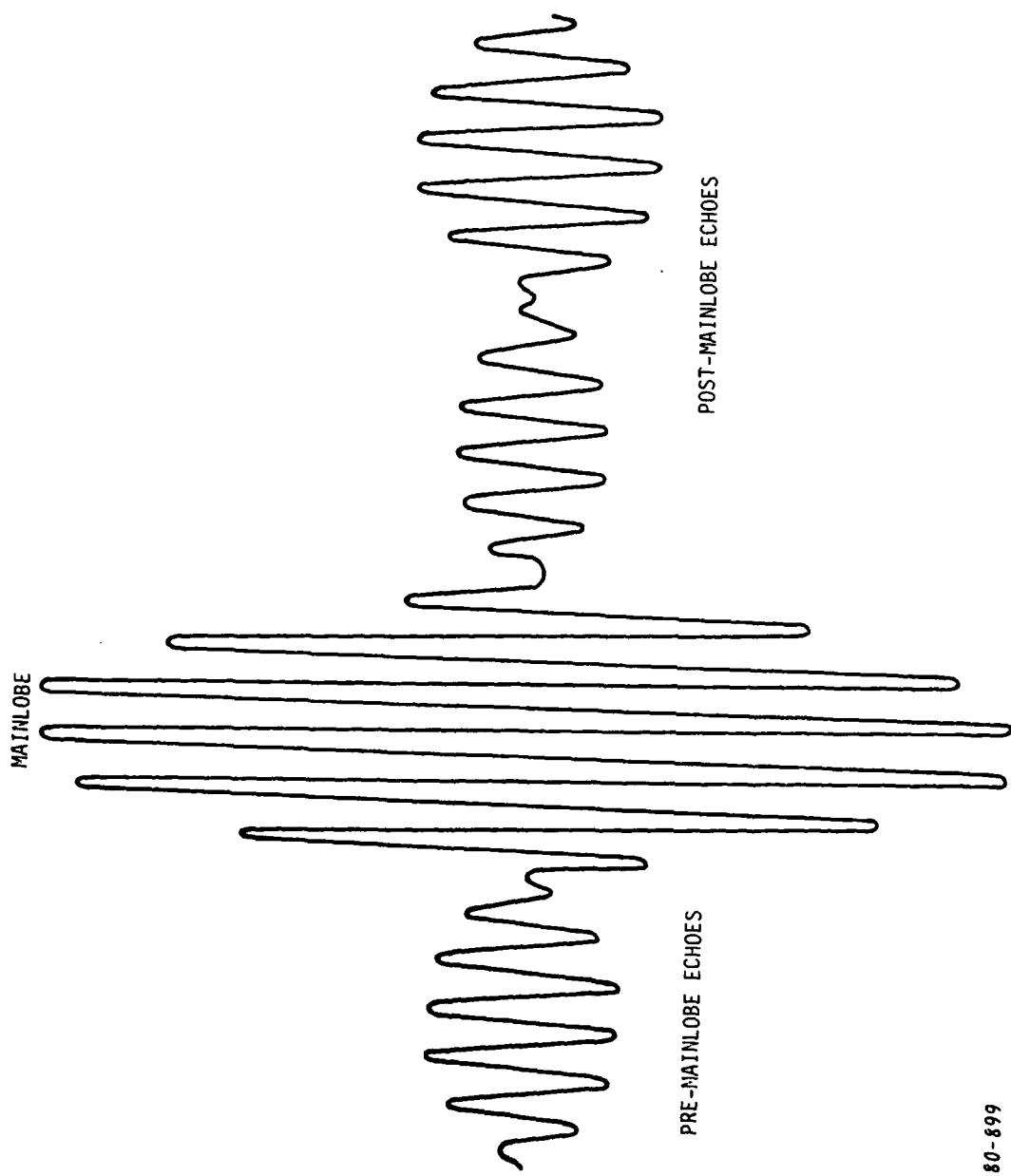
Hence, in order to achieve a 40-dB side-lobe level in a system with only amplitude distortion, the value of $\frac{a_n}{a_o}$ must not exceed 0.02 (or 0.17 dB).

The corresponding value of b_n in a system with only phase distortion must not exceed 0.02 radians or 1.14 degrees. For the general case with both

amplitude and phase distortion, and with $\frac{a_n}{a_o} = b_n = 0.01$, the corresponding values are 0.09 dB and 0.57 degree, respectively. It should be noted that a 40-dB side-lobe level is extremely difficult to obtain without equalization, since the amplitude and phase distortion of typical microwave components are generally greater than the values given in the example.

The MTE was designed to cancel the parasitic time side lobes, appearing at its input, by generating its own artificial equalizer side lobes, whose envelopes are properly delayed (or advanced) to coincide in time with the parasitic side lobes. In addition, the amplitude and phase of each artificial side lobe can be separately adjusted to produce an equal amplitude phase reversed replica of the corresponding parasitic side lobe.

Generation of the equalizer echoes is accomplished by tapping off portions of energy from the main signal lobe on the main transmission path, directing these portions through properly adjusted delay lines, and reintroducing the delay signal portions back into the main transmission path with proper amplitudes and polarity. The time domain output response of the MTE is shown in Figure 2.



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Figure 1. Time Side-Lobe Distortion

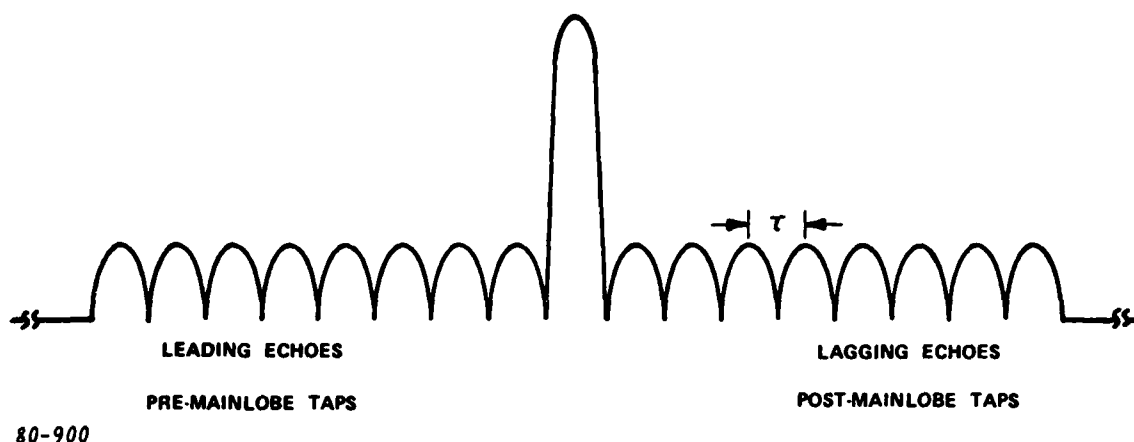


Figure 2. Time Domain Output of Microwave Transversal Equalizer

To obtain the proper amplitude and phase/time delay levels, the following must be considered.

1.1 AMPLITUDE

A normalized uncorrected voltage level (V_u) corresponding to an uncorrected side-lobe power level (P_u) is given in the following expression:

$$P_u = 20 \log (V_u) \quad (4)$$

Equation 4 is used to compute a value of 0.126 for V_u with an uncorrected side-lobe echo level of -18 dB. A correction voltage (V_c) of the proper amplitude and phase is required to reduce V_u to the desired equalized level (V_e) corresponding to a power level (P_e) of -35 dB, where:

$$V_c = V_u - V_e \quad (5)$$

and

$$P_e = 20 \log (V_e) \quad (6)$$

The defined distortion equalization is shown in Figure 3. Equation 6 is used to compute a V_e of 0.010 for the indicated level of P_e . A normalized correction voltage of 0.116 is calculated with equation 5, and the corresponding correction relative power level is -18.7 dB. A continuous range of amplitude adjustments is provided by variable PIN attenuators which are located in each of the 16 required taps.

1.2 PHASE/TIME DELAY

The required time delay (τ) per tap for a given RF bandwidth (B) is given by:

$$\tau = \frac{1}{B} \quad (7)$$

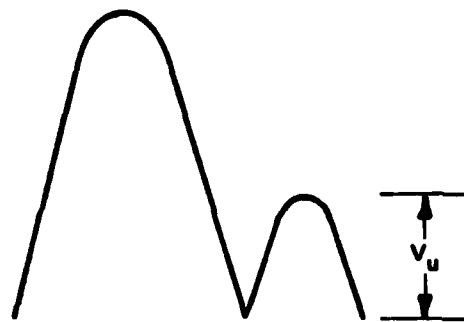
The number of cycles (n) in a time side lobe is a function of the RF period (T) corresponding to a center frequency (F), where:

$$n = \frac{\tau}{T} \quad (8)$$

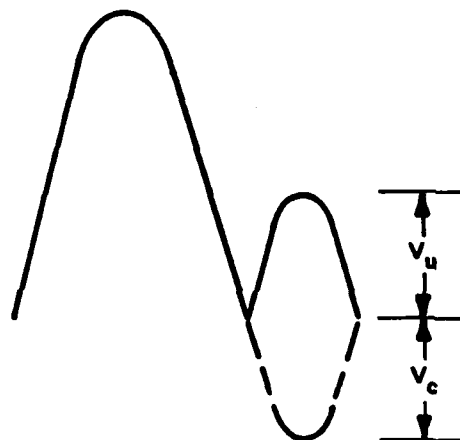
$$T = \frac{1}{f} \quad (9)$$

for $B = 300$ MHz and $f = 3.3$ GHz. Equations 7 through 9 are used to compute a required time delay (or tap spacing) of 3.3 ns, containing 11 RF cycles with a period of 0.303 ns. In order to effect echo cancellation, the MTE must contain a variable time delay in each tap with an adjustment range of $1/2$ wavelength ($\lambda/2$), or 180 degrees, or 0.15 ns. A continuously variable line stretcher is included in each tap arm to perform this function.

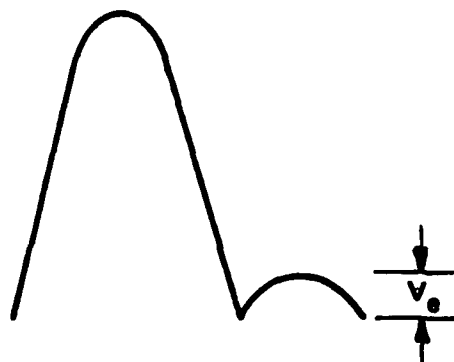
Amplifiers are included in both the mainline and decoupled arms (taps) to overcome the circuit losses.



A. UNEQUALIZED VOLTAGE LEVEL



B. SUMMATION WITH CORRECTION VOLTAGE



80-901 C. EQUALIZED VOLTAGE LEVEL

Figure 3. Distortion Equalization

2. GENERAL DESCRIPTION

A Microwave Transversal Equalizer (MTE) shown in Figure 4 is used to equalize both amplitude and phase distortion of various microwave components and devices. The MTE generates a well-controlled train of echoes, obtained by:

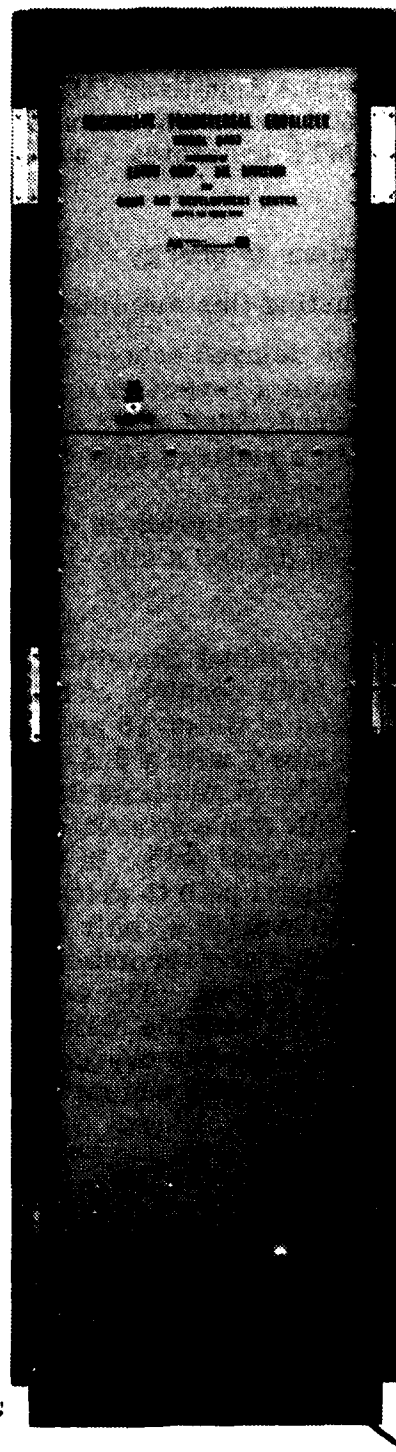
- Tapping off portions of energy from the main signal
- Individually adjusting this amplitude and phase
- Reintroducing the delayed echoes into the main signal path to approximate a reversed replica (equal amplitude and 180-degree phase shift) of the distorted side lobe and result in a reduced side-lobe distortion level.

The MTE designed for this program is capable of reducing a side-lobe level of -8 dB to less than -34 dB and a side-lobe level of -18 dB to approximately -40 dB.

An open view of the RFI cabinet containing the MTE system is shown in Figure 5. Basically, the MTE consists of four mainline delay circuits to generate the train of 32 echoes of which 16 are from Section A (pre-lobe) and 16 are from Section B (post-lobe), with a 3.3-ns time delay between echoes of each train. The amplitude level and time delay (phase) of each echo is individually adjusted with a PIN diode attenuator and variable delay line (line stretcher) included in its own signal path. In addition, a 56.1-ns delay cable is included in the Section B signal path to produce the required post-lobe echoes. Although 32 taps are available, only 16 are used simultaneously. Therefore, the developed echoes are recombined in two eight-way combiners to produce a single train of 16 echoes. The echoes are amplified to overcome their circuit losses, recombined with the mainline lobe in a two-way combiner, and further amplification is provided to overcome the overall MTE losses. A detailed description of the components and measured characteristics are given in the following sections.

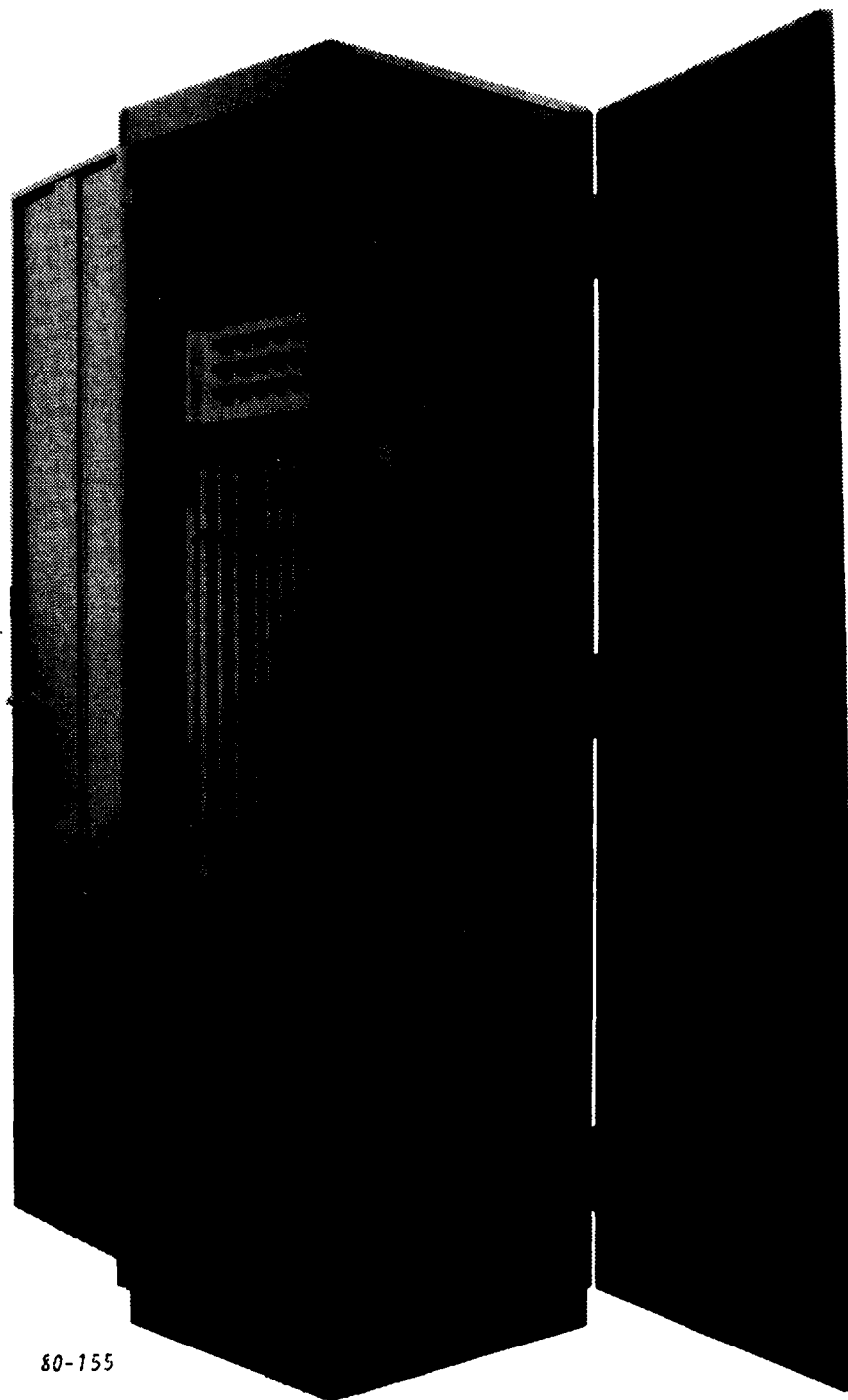
2.1 MAINLINE DELAY CIRCUIT

A mainline delay circuit, shown in Figure 6, is the equivalent of a microwave tapped delay line providing 20-dB decoupling taps, with 3.2-ns spacing between taps. The circuit provides for eight decoupled taps, four from Section A (pre-lobe) and four from Section B (post-lobe). The tap separation (delay) is provided by a fixed length of line connected in cascade with the couplers. The straight line fixed delay circuit configuration was chosen to minimize the number of bends per section and ensure optimum VSWR (minimum induced distortion).



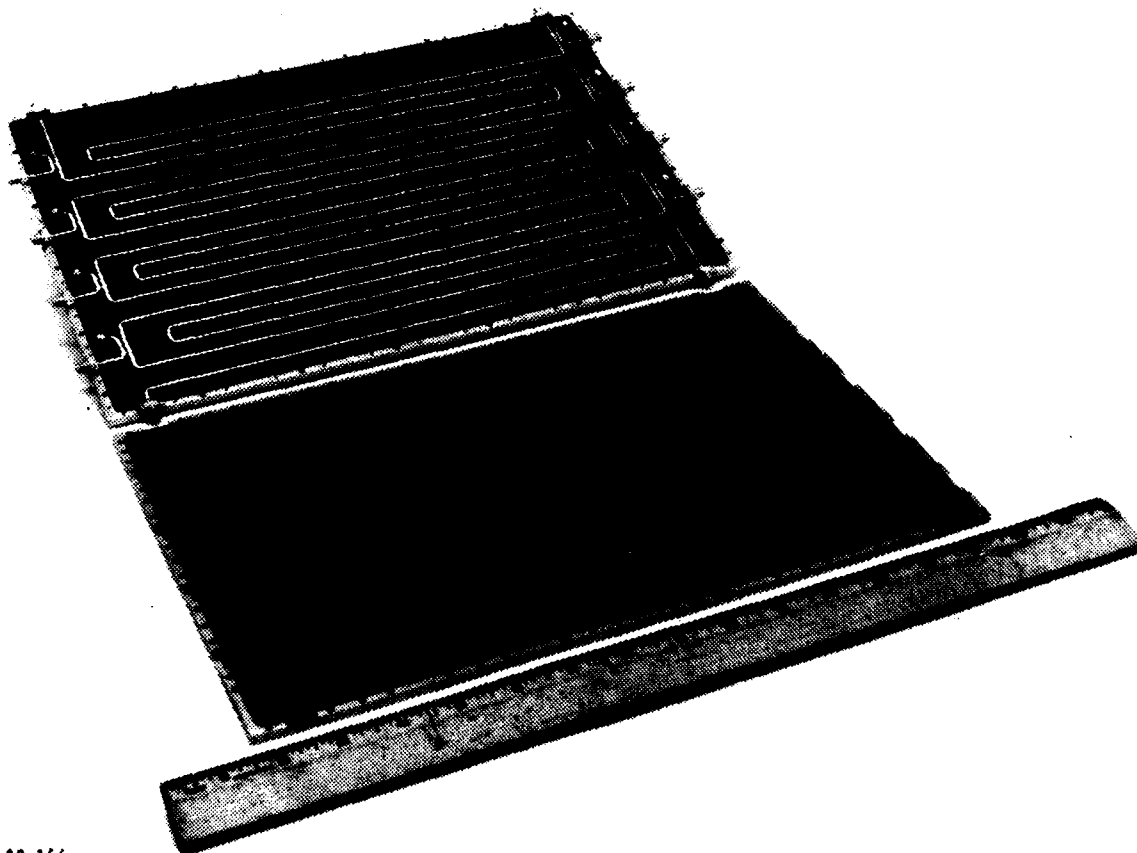
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Figure 4. Microwave Transversal Equalizer



80-155

Figure 5. Open View of MTE-RFI Cabinet



80-156

Figure 6. Mainline Delay Circuit

Measured data of the delay circuit resulted in an insertion loss of 2.8 dB (Figure 7) and an input/output VSWR = 1.38:1 (Figure 8). Each tap provided 21-dB decoupling and a 3.10 ± 0.15 ns delay between taps.

To obtain 32 taps, four mainline delay circuits are used in the MTE system and the measured data is typical for all four units.

2.2 VARIABLE ATTENUATOR

The variable attenuator permits the MTE to provide pre-lobe and post-lobe signal levels of various amplitude to cancel amplitude distortion. The attenuators were designed, fabricated, and tested at AIL to optimize the attenuator operating characteristics thereby ensuring minimum induced MTE system distortion.

The attenuator employs eight PIN diodes mounted in a microstrip configuration with alumina as the substrate. The input/output VSWR is optimized with the use of matching networks and a constant current control circuit is provided for each attenuator. Measured data shows that for an attenuation change of 35 dB, the variation is less than 0.6 dB over the operating frequency range. Furthermore, the VSWR is less than 1.38:1 and the induced time delay variation is approximately 0.1 ns for all values of attenuation. Figure 9 shows the measured attenuation values from 3.0 to 3.5 GHz as the total diode current is varied from 0 to 4 mA. Since the MTE system requires 17 attenuators, for ease of fabrication, six attenuator circuits are mounted in a single housing unit as shown in Figure 10. The control panel, containing the constant current source circuits, is shown in Figure 11.

2.3 PHASE/TIME DELAY ADJUSTERS

Variable time delay adjustment for the MTE is obtained by employing commercially available coaxial line stretchers in each tap and mainline signal path. The line stretcher is capable of providing 1-ns delay which is sufficient to meet the MTE requirement and also compensate for slight delay variations in the mainline/tap signal circuitry. Figure 12 shows the line stretchers mounted in the MTE RFI shielded cabinet. A calibrated indicator, in 0.1-ns steps, is provided on each line stretcher for ease of tuning and re-setability.

2.4 POWER COMBINERS

The combining of the tap and mainline signals is provided by the use of two-way and eight-way resistive power combiners. The circuit is fabricated in a stripline configuration using Duroid as the dielectric material.

Measurements of the VSWR in the two-way and eight-way combiners show a maximum of 1.35:1 for all input and output ports. The insertion loss

for the two-way combiner is approximately 3.2 dB and both ports track within 0.1 dB of each other.

Insertion loss measurements of the eight-way combiner resulted in a 9.3-dB loss and less than 0.1-dB variation from port-to-port over the operating frequency range. No measurable delay occurs from port-to-port on either combiner. Figure 13 shows the eight-way combiner circuit and its housing.

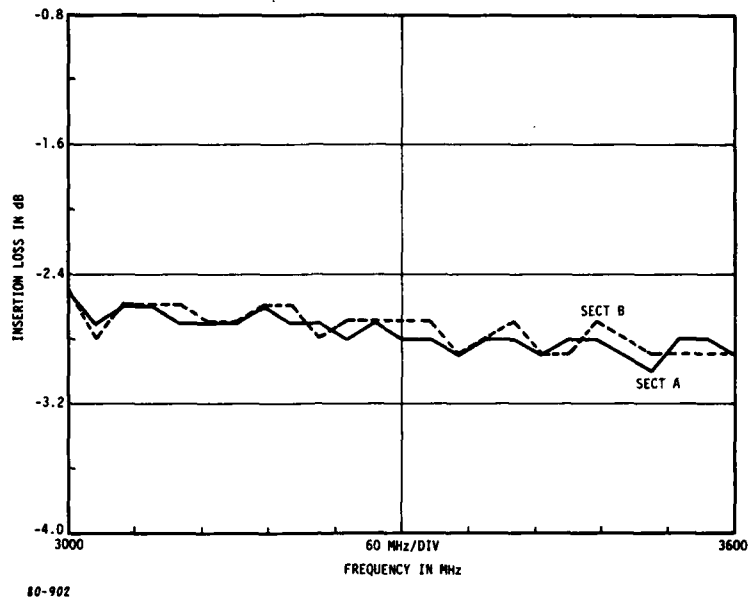


Figure 7. Measured Insertion Loss of Mainline Delay Circuit

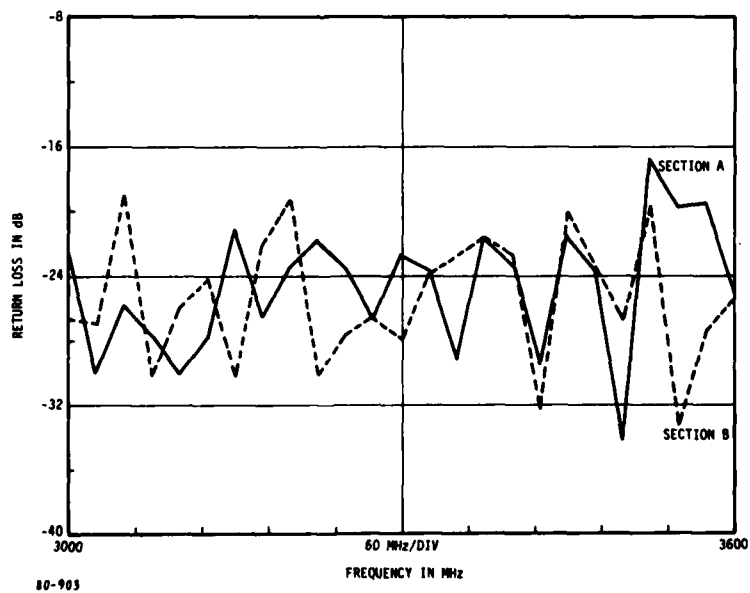


Figure 8. Measured Return Loss (VSWR) of Mainline Delay Circuit

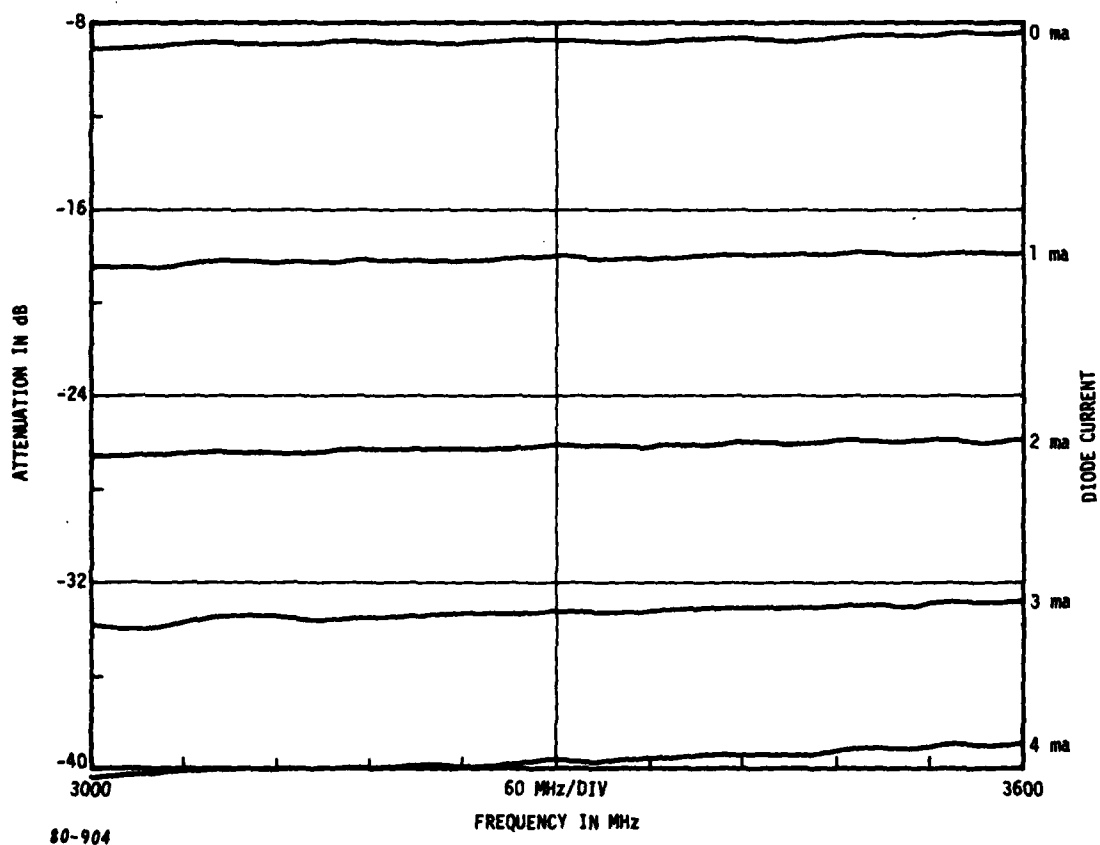


Figure 9. Measured Diode Attenuation Versus Frequency With Diode Current as a Parameter

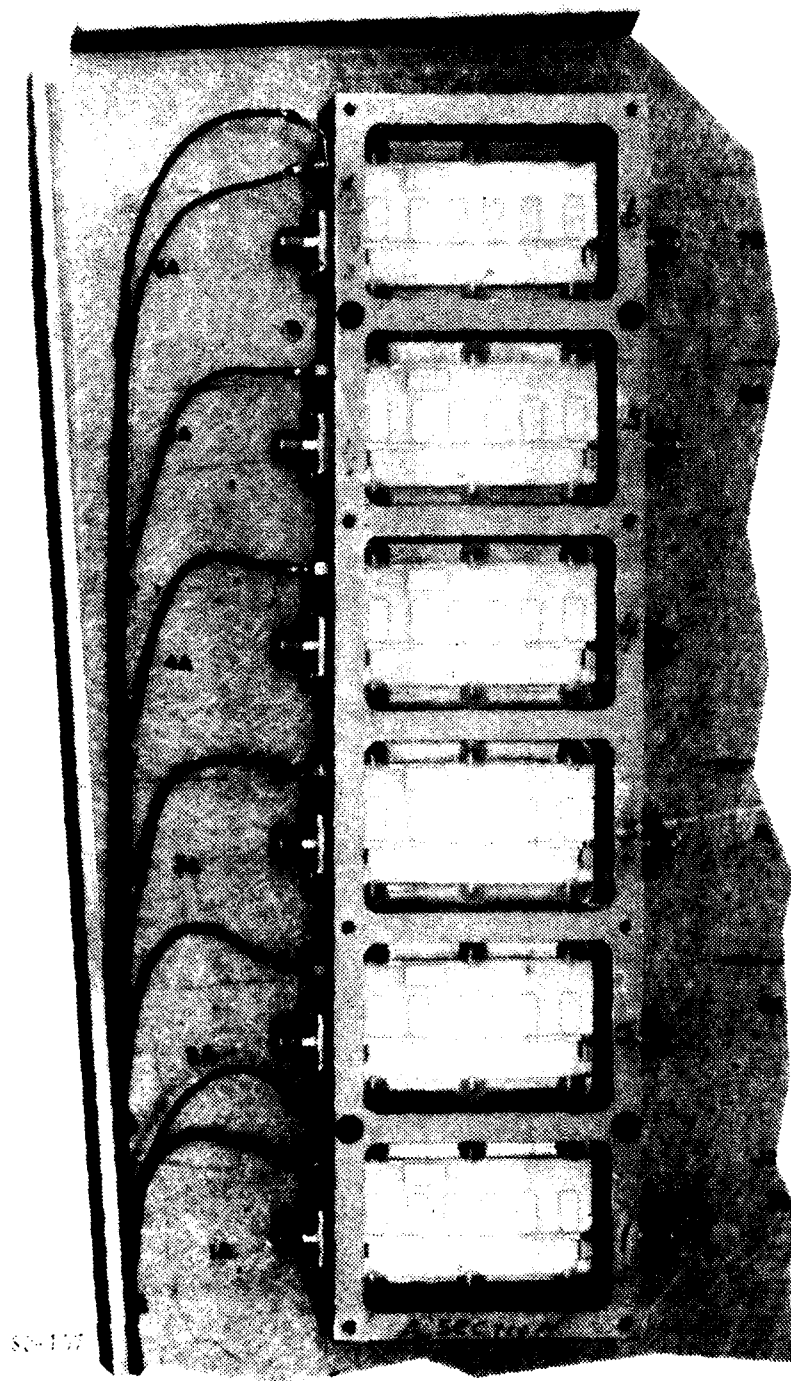
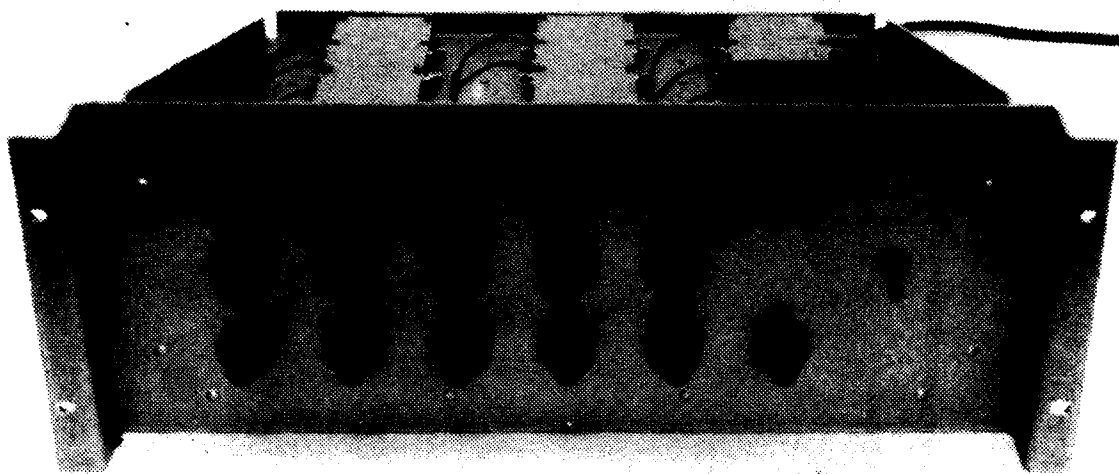


Figure 10. PIN Diode Attenuator



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Figure 11. Control Unit for Diode Attenuators

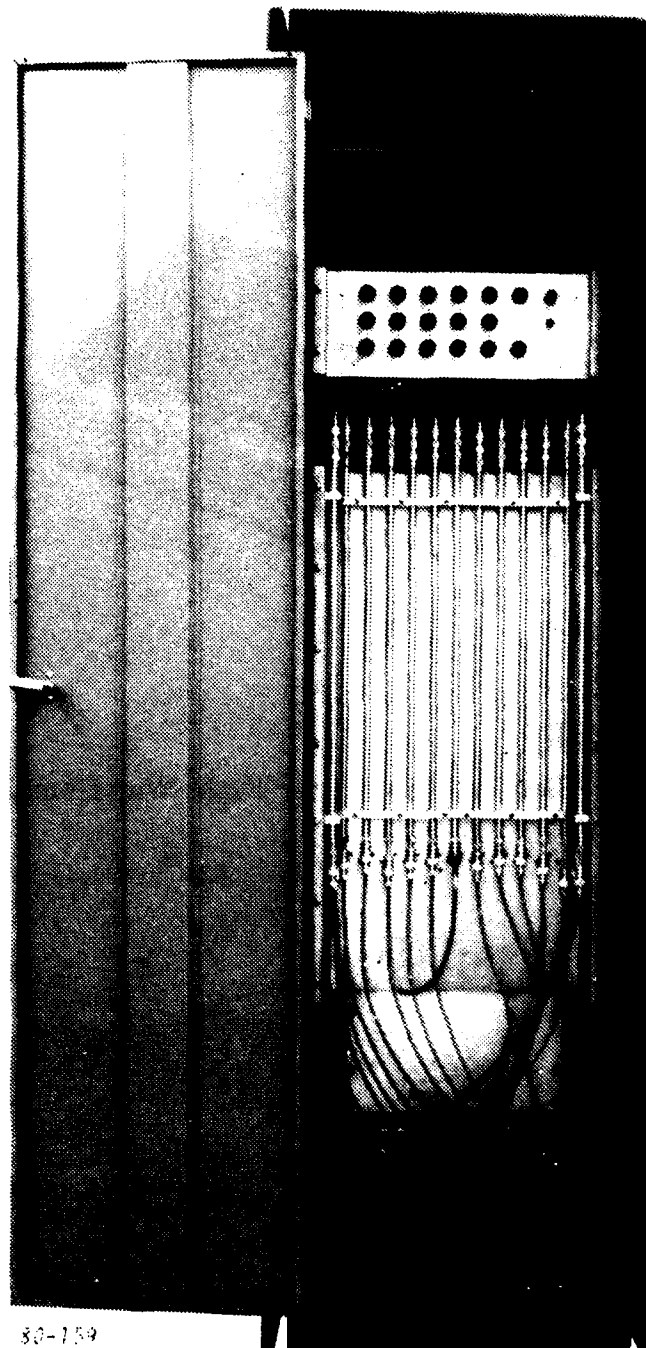
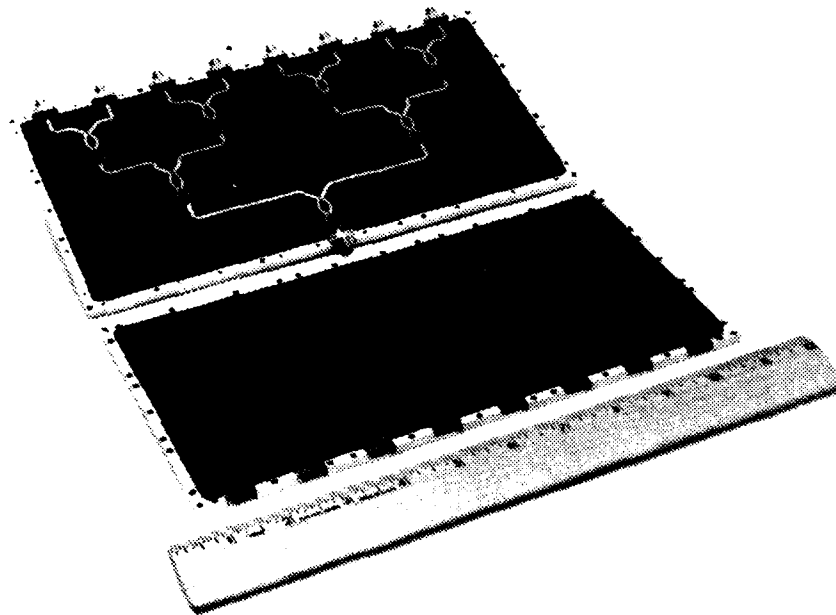


Figure 12. Time Delay Adjusters (Line Stretchers) Mounted in MTE System



80-180

Figure 13. Stripline Circuit for Eight-Way Combiner

3. MTE SYSTEM PERFORMANCE

The MTE is capable of operating over any 300-MHz bandwidth in the 3.0 to 3.5 GHz frequency range. Figure 14 is a block diagram of the MTE system, and shows the components employed and the availability of 32 taps of which 16 can be used simultaneously. The pre-lobe taps are designated as 1A to 16A and the post-lobe as 1B to 16B.

Based on the evaluation of the measured data of the individual components, measurements were carried out to exhibit the performance of the MTE system.

The characteristics of the MTE are as follows:

Operating frequency range	3.05 to 3.5 GHz
Input/output VSWR	1.1:1 maximum
Spurious response	<-60 dBm for +10 dBm input
Output noise level (50-ohm input)	-60 dBm for BW = 1 MHz
Repeatability variation	no noticeable change per adjustment
Stability variation	<0.1 dB change (24-hour period)

3.1 MTE SYSTEM TIME DOMAIN MEASUREMENTS OF AMPLITUDE AND TIME DELAY

The MTE time delay and attenuator adjustment range was measured by using the test setup shown in Figure 15. As can be seen, a pulsed RF signal is applied to the MTE input and the output signal, given in Figure 16, consists of a series of pulses from the mainline path and 16 taps. The time delay between pulses is fixed at 3.3 ns by the mainline delay and initial setting of the line stretchers. The amplitude has been adjusted by the attenuators for an equal output level of -17 dB below the mainline signal level. To ensure the required 0.15-ns delay and 20-dB attenuation range, each tap control was adjusted and the results are given in Table 1. As can be seen, a delay variation of 1 ns and an amplitude range of 0 to 30 dB was achieved for each tap which will exceed the requirements of this program.

3.2 SIDE-LOBE DISTORTION MEASUREMENT

The test setup given in Figure 17 was used for the side-lobe distortion measurement at the RADC facility. An initial measurement was performed with a side-lobe distortion extending over a pre-lobe time domain of 7 ns. Adjustments of taps 1A through 8A inclusive were performed and the distorted output side lobe was reduced to >45 dB.

A further test was performed by injecting an artificial side-lobe distortion (tap 10A) to occur at an arbitrary tap (6A) whereby side-lobe reduction could be demonstrated. For an injected side-lobe level of -8 dB, tap adjustments of phase and amplitude resulted in a side-lobe reduction to -35 dB. For an injected side-lobe distortion level of -17 dB, the side lobe was reduced to a -40 dB level. The measured data is given in Figure 18.

TABLE 1. TIME DOMAIN MEASUREMENT OF DELAY AND AMPLITUDE CONTROLS

Input: Pulsed RF signal

Output: Side-lobe attenuation and time delay variation

Tap no.	Line stretcher set at	Time delay (ns)	Side-lobe level (dB)
1A	7.95	3.4 < 3.1 minimum 4.1 maximum	-17 + Δ
2A	6.2	3.3 < 2.8 minimum 3.9 maximum	-17 + Δ
3A	3.7	3.4 < 2.6 minimum 3.6 maximum	-17 + Δ
4A	1.5	3.4 < 3.3 minimum 4.2 maximum	-17 + Δ
5A	9.1	3.4 < 3.3 minimum 4.2 maximum	-17 + Δ
6A	7.5	3.2 < 2.9 minimum 3.9 maximum	-17 + Δ
7A	7.0	3.2 < 2.9 minimum 3.9 maximum	-17 + Δ
8A	6.1	3.2 < 2.8 minimum 3.8 maximum	-17 + Δ
M	4.1	Reference	-17 + Δ
1B	1.2	3.5 < 3.4 minimum 4.5 maximum	-17 + Δ
2B	3.7	3.3 < 2.9 minimum 3.9 maximum	-17 + Δ
3B	5.2	3.5 < 2.9 minimum 3.9 maximum	-17 + Δ
4B	7.2	3.5 < 2.6 minimum 3.6 maximum	-17 + Δ
5B	0.5	3.5 < 3.4 minimum 4.5 maximum	-17 + Δ
6B	1.4	3.3 < 3.0 minimum 4.0 maximum	-17.5 + Δ
7B	3.2	3.1 < 2.9 minimum 3.9 maximum	-17 + Δ
8B	6.2	3.4 < 2.6 minimum 3.7 maximum	-17 + Δ

Data taken at minimum attenuation (-17 dB)

Δ = 0 to 30 dB ±0.5 dB

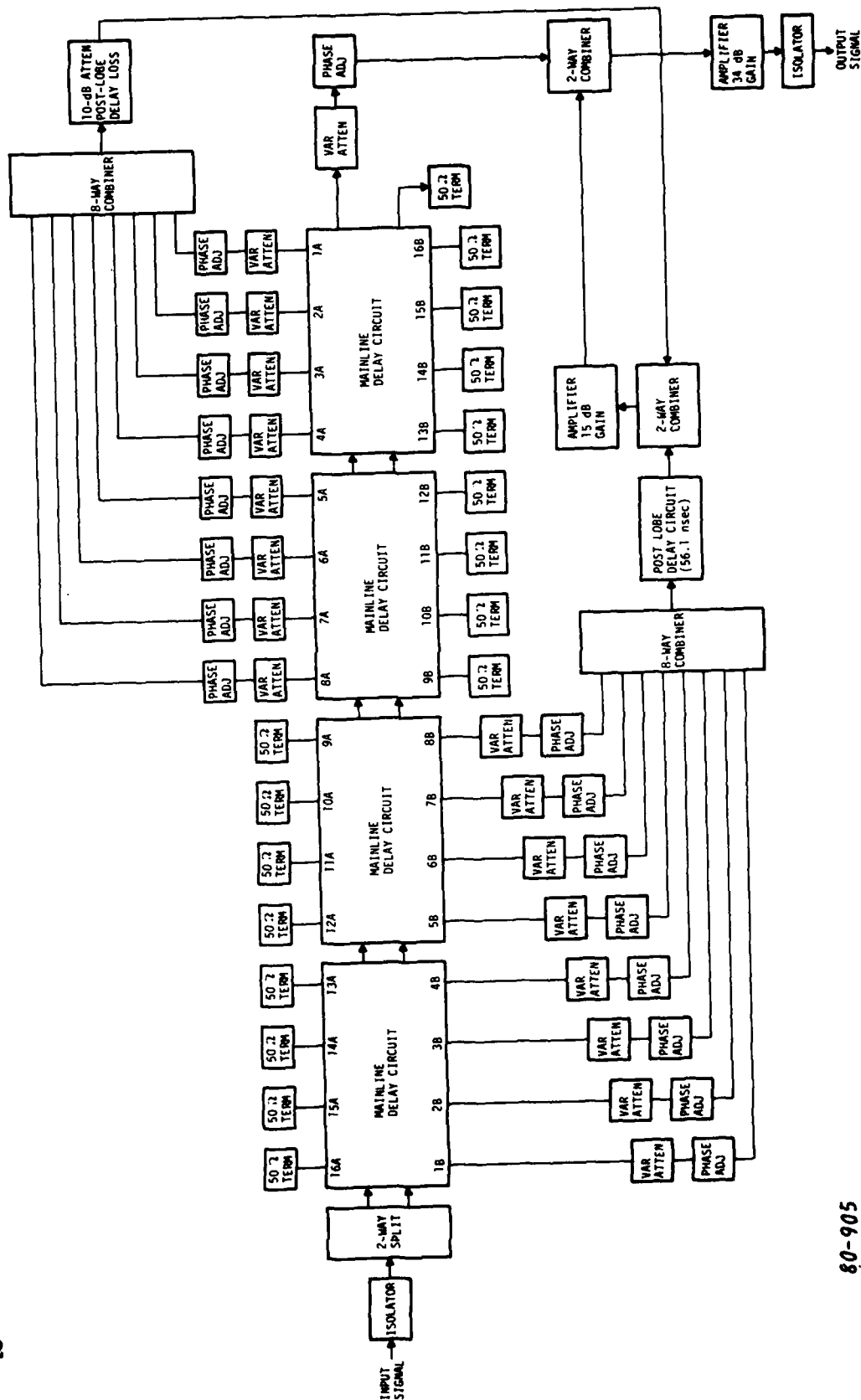
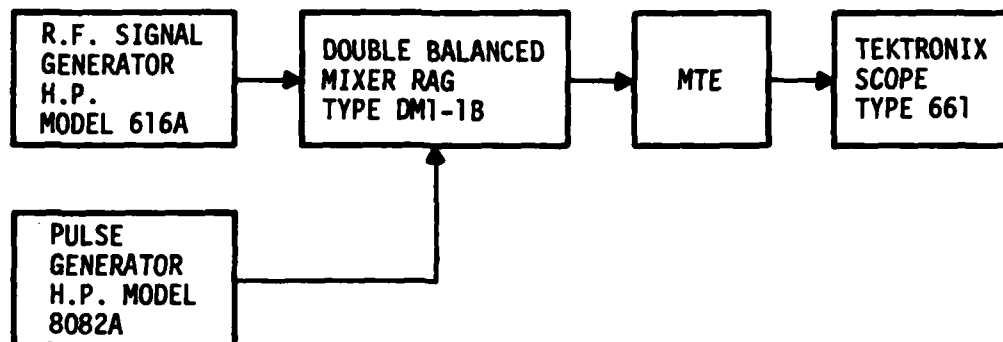


Figure 14. Block Diagram of Microwave Transversal Equalizer



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Figure 15. Test Setup for MTE Time Domain Measurement

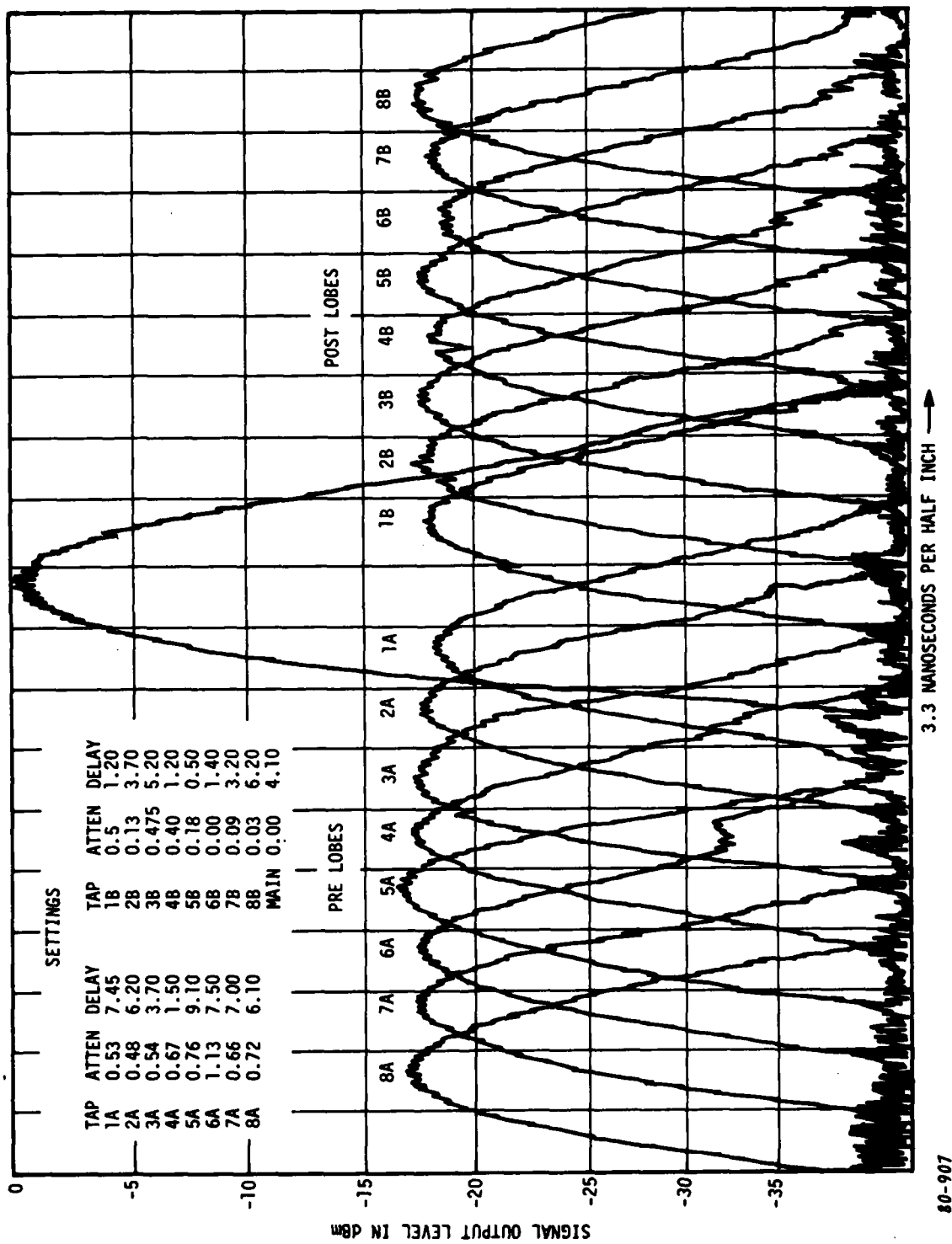
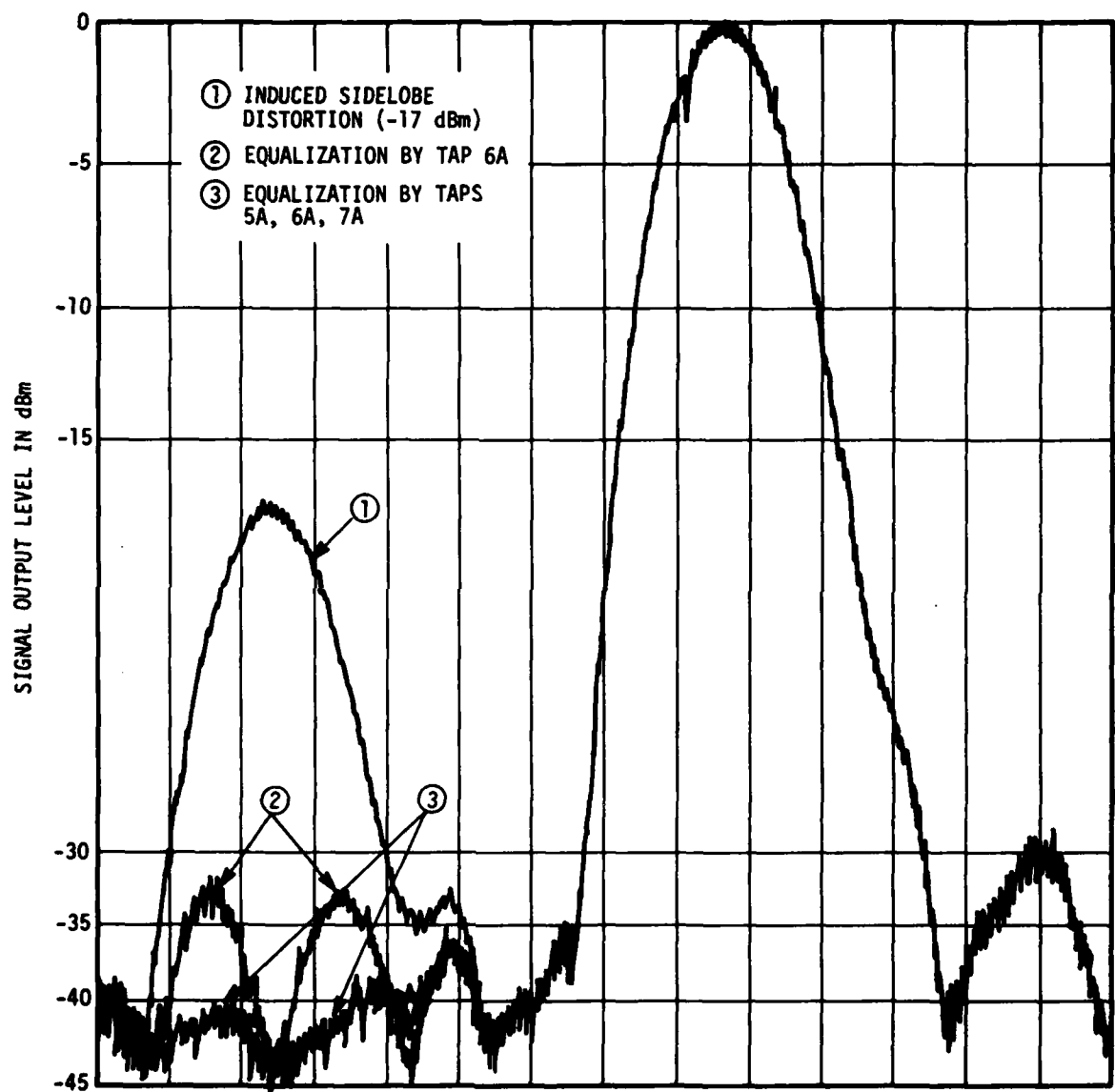


Figure 16. MTE Output Signal in Time Domain



80-909

Figure 18. Measured Side-Lobe Equalization for -17 dBm Input Distortion Level

4. CONCEPTUAL DESIGN FOR AUTOMATING THE MTE

In order to automate and adaptively control the MTE, the following task efforts will be required:

- (1) A sampling technique must be developed to determine the system distortion levels.
- (2) A minicomputer, such as the HP 2100 or equivalent, is needed in order to rapidly determine the phase and amplitude control element settings required to minimize the measured distortion.
- (3) An algorithm must be developed to accomplish computer control.
- (4) Suitable electronic circuitry must be designed to interface between the computer and the MTE, thereby permitting adaptive control.
- (5) Suitable variable time delay components/structures must be developed and fabricated to facilitate adaptive phase control.
- (6) The MTE must be modified to facilitate installation of the aforementioned time delay components and the electronic control circuitry.

The following discussion will therefore consider the preliminary tasks 4 and 5.

4.1 INTERFACE ELECTRONICS

The present MTE is manually controlled by individual and separate adjustment of amplitude (attenuation control) and phase (time delay). Amplitude adjustment with PIN diode attenuators is accomplished with potentiometer adjustment of analog voltages for each equalizer tap (open loop control).

In a closed-loop adaptive equalizer system, an analog-to-digital (AD) converter will be required to digitize the signal in either the frequency or time domain. The AD converter will digitize the analog waveform at a rate high enough to yield an accurate representation for subsequent processing. As an example, a 32-lobe pulse of 300- μ s duration would permit about nine digitizations per lobe assuming one digitization per microsecond. Nine per

lobe is probably an adequate number. A shorter duration pulse would probably necessitate a faster AD. Since the HP 2100 would not be able to accept words faster than a 1-MHz rate, a high-speed buffer memory would then accept the AD output and in turn output the information to the HP 2100.

Assuming a 40-dB spread in amplitude, an eight bit logarithmic converter yields 0.15-dB resolution. Eight bits is a standard AD word size, and 0.15-dB resolution is considered by AIL to be quite adequate for the intended application.

Words outputted from the computer to the DA's would drive an automated adaptive equalizer and must provide sufficient resolution for proper attenuator and time delay control. The basic word size of the HP 2100 is 16 bits, and a preliminary analysis by AIL indicates that this word size easily satisfies the most stringent resolution requirements envisioned for attenuator and time delay control.

4.2 COMPUTER/EQUALIZER INTERFACE

Figure 19 shows a straightforward but expensive computer/equalizer control interface. The figure assumes analog control of the attenuators and time delay devices in the equalizer. A less expensive method would include a single high speed DA followed by 64 sample/hold circuits, one for each control line. Each sample/hold would, of course, need to be periodically refreshed. Also, the 64 registers would need to be multiplexed to the DA.

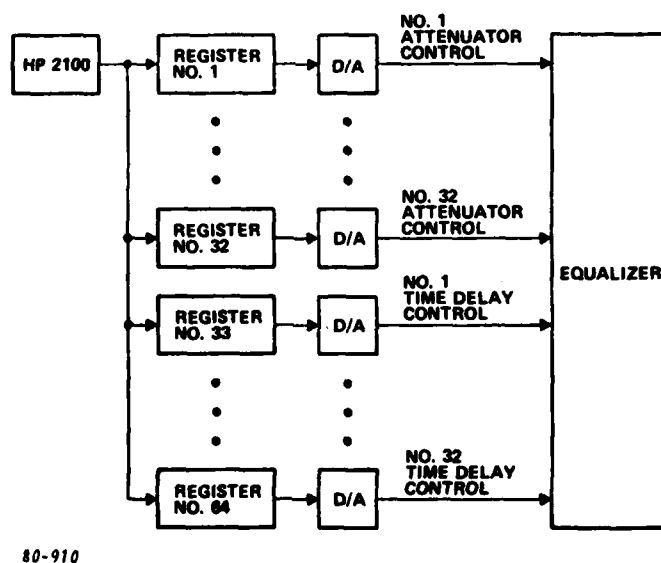


Figure 19. Computer/Equalizer Interface (32 Lobes)

4.3 PIN-DIODE STEPPED TIME DELAY

A solid-state adjustable time delay device is required for each tap in order to shift the artificial echo over a minimum range of 0 to 0.15 ns. This range will allow alignment of the artificial echo within 180 degrees of the distortion echo carrier phase in order to provide cancellation of signals with proper amplitude levels.

A review by AIL of existent components has not revealed any suitably available commercial devices. Other types of related devices were examined including solid-state phase shifters and microwave acoustic bulk wave delay structures. Preliminary analysis of these devices reveals that they are unacceptable for the intended application because the solid-state phase shifter does not exhibit true time delay over the required range, and the microwave acoustic delay line exhibits excessive time delay ($>1 \mu\text{s}$) as well as excessive insertion loss ($>10 \text{ dB}$).

A preliminary review of possible time delay configurations has not disclosed any continuously variable voltage-controlled devices. The program objectives, however, can be satisfied with stepped delay devices. A preliminary analysis has indicated that such devices are practical, and a number of possible configurations are shown in Figure 20. The devices are basically either transmission type or reflective type structures, which use the conduction state of the PIN diodes to alter the length of a transmission line. The necessary line lengths to satisfy the time delay increments of 0.01 ns are given in wavelength λ as:

$$\lambda = T \times \frac{v}{\sqrt{\epsilon}} \quad (10)$$

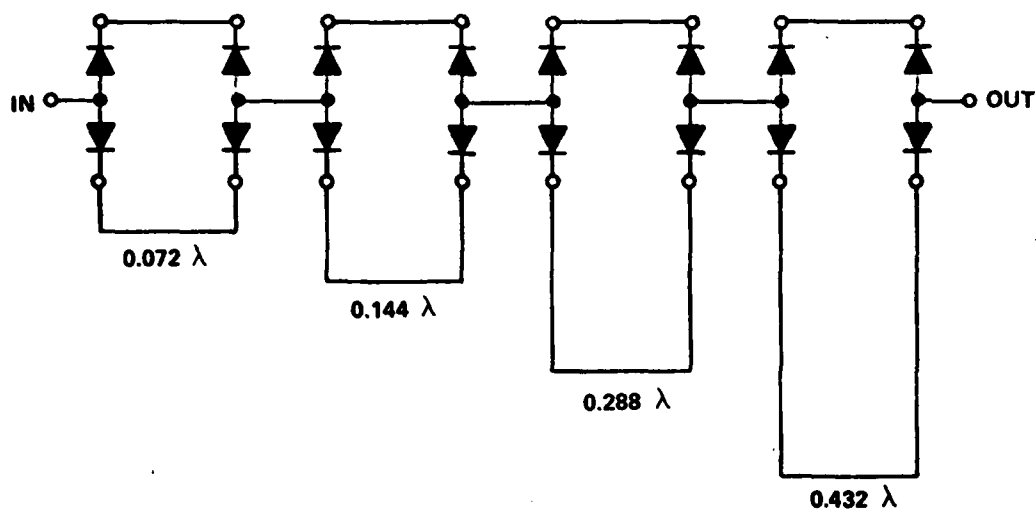
where:

v = velocity of propagation in air (11.8 inches/ns)

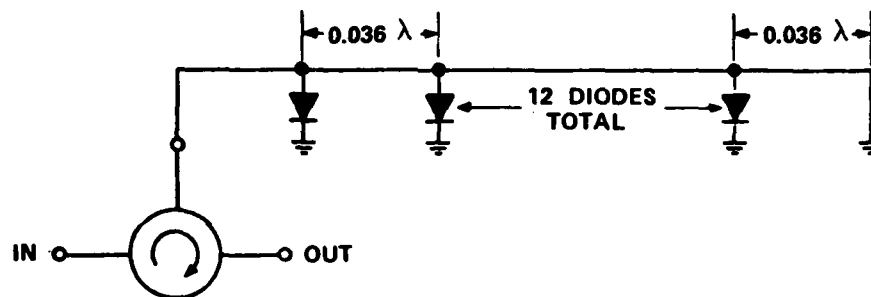
ϵ = dielectric constant of transmission line

The smallest diode spacing shown (0.036λ) is 0.038 inch in a stripline structure with $\epsilon = 2.5$, and such configurations can be accomplished in the AIL microelectronics laboratory facility.

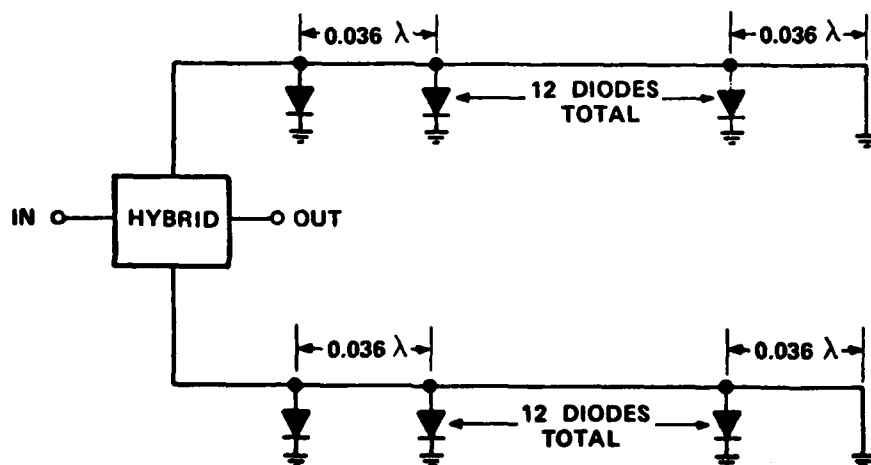
Figure 20B and 20C are equivalent circuits; however, the increased quantity of diodes (24 total) in the hybrid coupled circuit, Figure 20C, may offset the cost of the circulator shown in Figure 20B. The alternate circuits of Figure 21 have been postulated in an attempt to reduce the number of diodes. Figure 21A (four diodes total) is equivalent to Figure 20A (16 diodes total);



A. SWITCHED LINE TIME DELAY



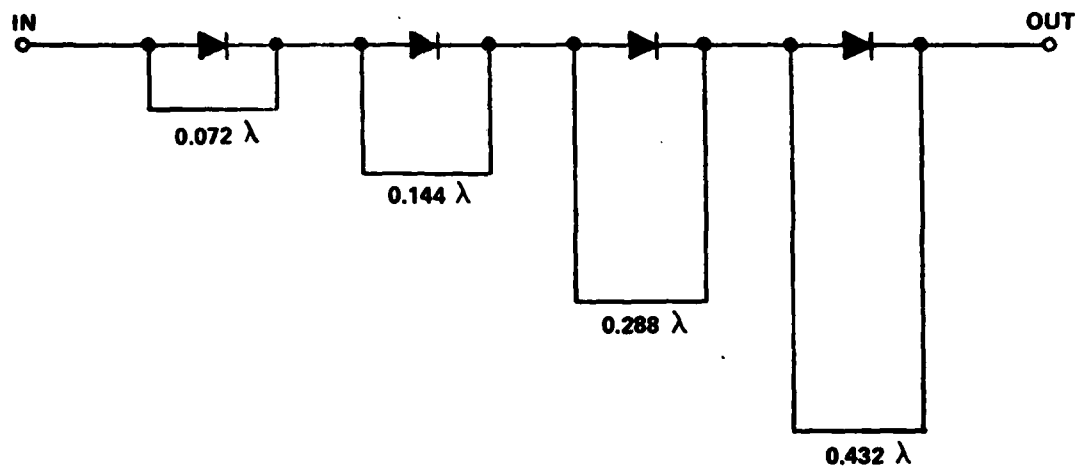
B. CIRCULATOR COUPLED REFLECTIVE TIME DELAY



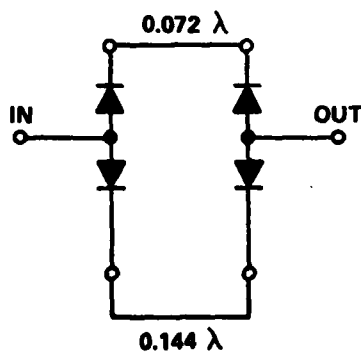
C. HYBRID COUPLED REFLECTIVE TIME DELAY

80-911

Figure 20. Variable Time Delay Devices



A. ALTERNATE SWITCHED LINE TIME DELAY



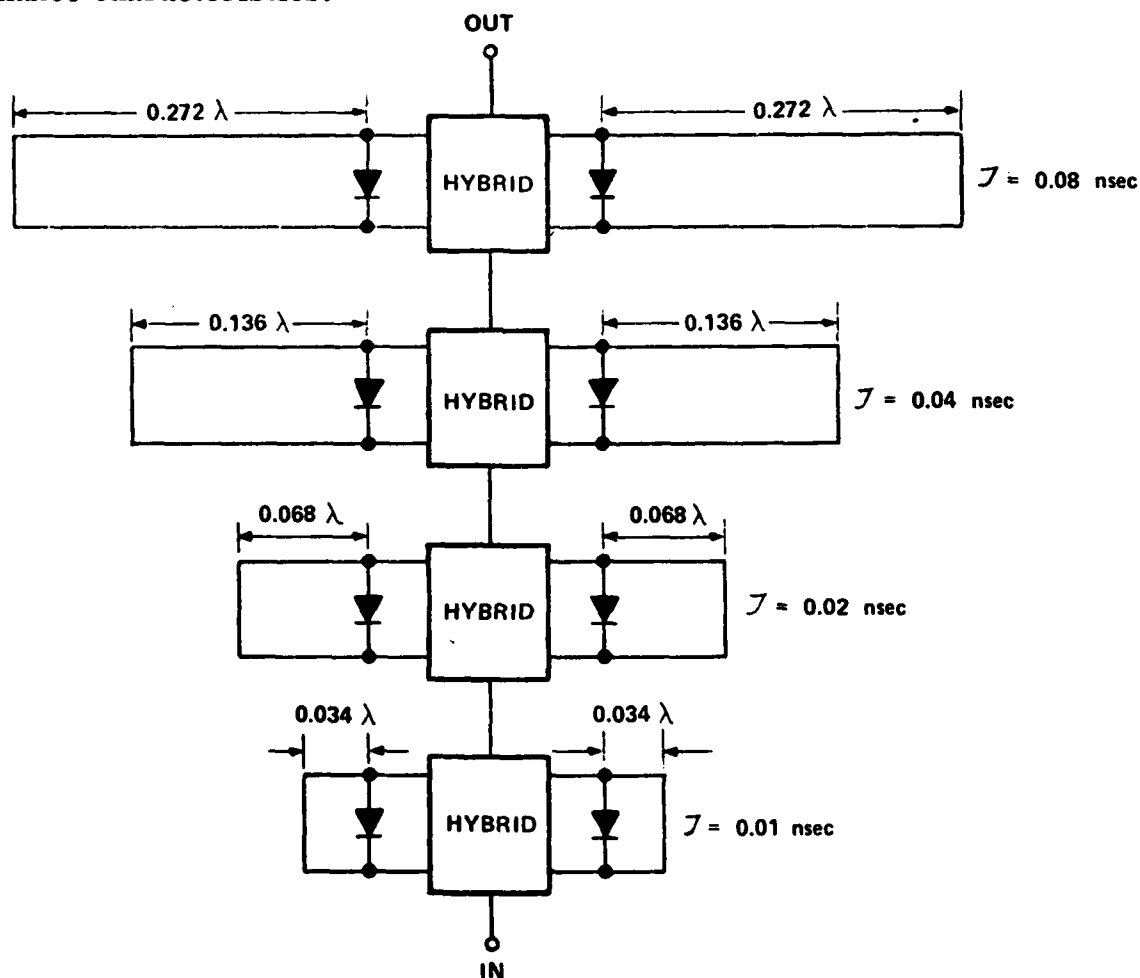
B. SERIES DIODE ARRANGEMENT

80-912

Figure 21. Alternate Switched Time Delay

however, the design implementation of Figure 21A may be difficult because of possible mismatch effects at the branch arms. Figure 20A may be converted from a series diode arrangement to a shunt diode arrangement with a reduction of four diodes. In addition, shunt diode arrangements are often easier to construct and require less sophisticated biasing arrangements. Finally, an attractive alternative to Figure 20C (24 diodes total) is shown in Figure 22 (eight diodes total). It should be noted that if the transmission line shorts shown in Figure 22 are replaced by diodes (eight additional), a 180-degree phase reversal circuit will be achieved, and minimum MTE cancellation capability will be substantially increased.

A preliminary analysis has been made of the alternate hybrid coupled effective time delay (Figure 22), in order to determine the expected performance characteristics.



80-913

Figure 22. 4-Bit Hybrid Coupled Reflective Time Delay

4.3.1 Frequency Considerations

For PIN diode operation as a practical stepped delay element at a given frequency (f), the carrier charge (Q_0) stored by the dc bias current (I_0) must be an order of magnitude greater than the carrier charge (Q_1) removed by the RF signal of peak current amplitude (I_1). The stated conditions are given in reference 2 and can be represented by the following expressions:

$$Q_0 = I_0 t \quad (11)$$

where the carrier lifetime (t) is a function of the PIN diode, and

$$Q_1 = \frac{I_1}{2\pi f} \quad (12)$$

where

$$I_1 = \sqrt{\frac{2P}{R_0}} \quad (13)$$

Preliminary design calculations have been carried out at a center frequency of 3300 MHz with the Crown DL-603 which has the following characteristics:

Carrier lifetime (t)	50 ns
Total capacitance (C_t)	0.3 pF
Series resistance (R_s)	0.6 ohm with 5 mA bias current
Parallel resistance (R_p)	>10 kilohms

With the PIN diodes operating at a center frequency of 3300 MHz in a 50 ohm (R_0) delay circuit at a power level (P) of 0 dBm, equations 11 and 12 yield the values of $Q_0 = 5 \times 10^{-10}$ (10 mA bias) and $Q_1 = 0.3 \times 10^{-12}$,

respectively. Since $Q_0 \gg Q_1$ the chosen PIN diode can be utilized as a time delay element in the desired frequency range.

4.3.2 Insertion Loss

The maximum insertion loss (L) of each hybrid section occurs with the shunt PIN diodes in a reverse bias condition. The one-way insertion loss is given (reference 3) by:

$$L = 10 \log \left[1 + \left(\pi f C_t R_o \right)^2 \right] \quad (14)$$

and predicts a loss of -0.1 dB/hybrid section. It should be noted that this value must be doubled to account for the two-way loss of the reflective device. In addition, the loss of the bias current elements (choke and blocking capacitors) is estimated to be 0.2 dB/hybrid section. The overall hybrid section loss is therefore 0.3 dB, and the total loss of the four cascaded hybrid sections is therefore estimated to be 1.2 dB.

4.3.3 Isolation

The minimum isolation (I) of each hybrid section occurs with the PIN diodes in a forward bias condition. The one-way isolation is given (reference 2) by:

$$I = 20 \log \left[1 + \frac{R_o}{2R_s} \right] \quad (15)$$

and predicts a one-way isolation of 32.6 dB. This value must also be doubled to account for the two-way transmission path of the reflective device. The second order echoes generated by the isolation effects of each hybrid are not time coherent, and the minimum isolation is therefore estimated to be -65.2 dB.

4.3.4 Stepped Delay Range

Figure 23 shows a 4-bit time delay device which is capable of 16 incremental time delay steps of 0.01 ns each. A transducer of this type could easily interface with the computer controlled 16-bit words to provide the desired adaptive operation.

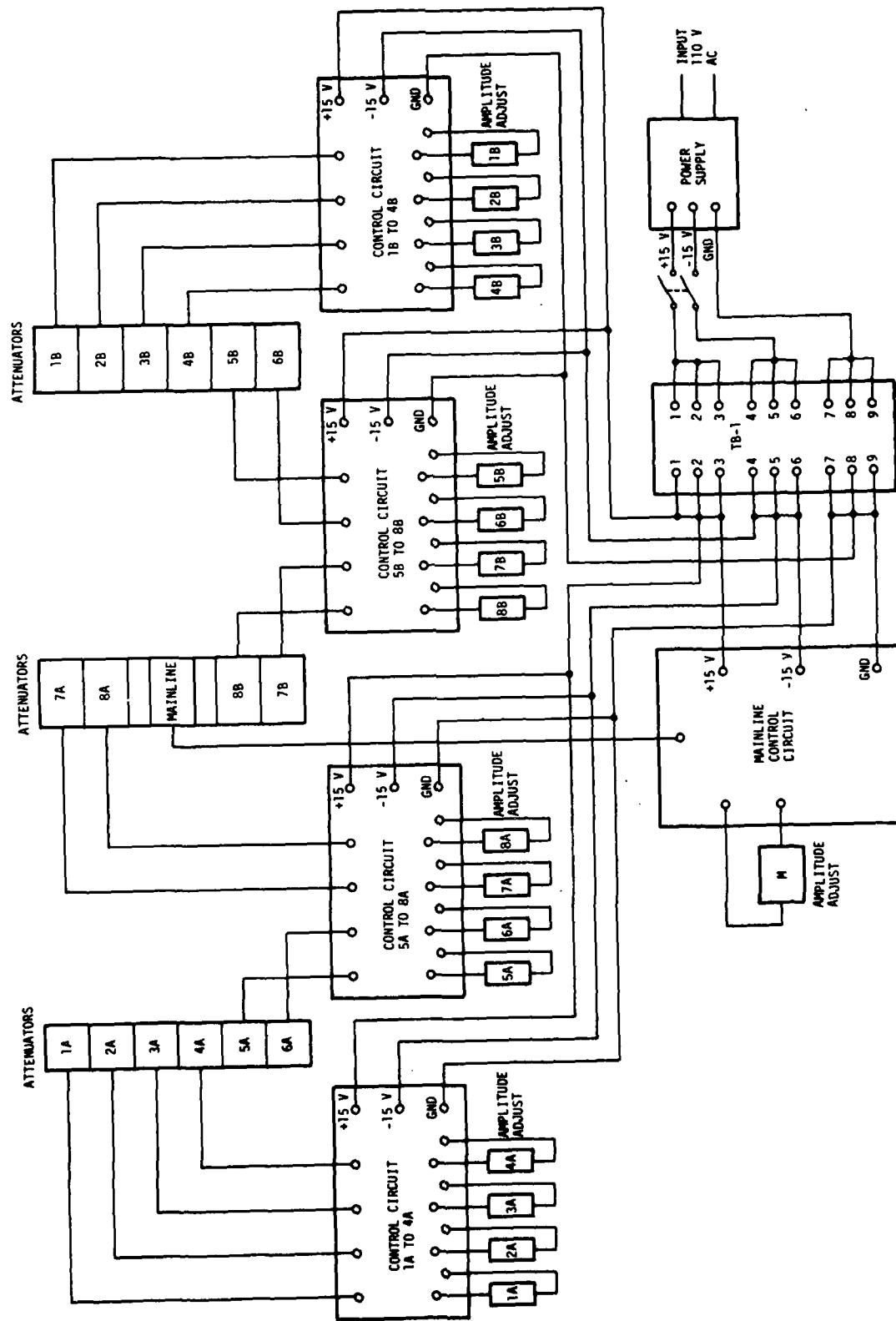


Figure 23. Wiring Diagram for Attenuator Control Unit

80-914

5. OPERATION OF MTE

The MTE generates a correction or equalization signal that will be used to cancel or reduce time side-lobe distortion introduced by one or more components in a microwave and/or radar system. The MTE provides equalization of 32 time side lobes (16 pre-mainlobes and 16 post-mainlobes) of which any 16 can be used simultaneously. Two adjustments (amplitude and time delay) are required for the equalization of each time side lobe and amplifiers are provided to overcome the MTE circuit losses.

The manual controls of the time delay and amplitude are located at the rear of the RFI cabinet (Figure 12).

The time delay of the correction signal is adjusted by varying the length of each line stretcher which has a range of 1 ns and is calibrated in 0.1-ns intervals.

The amplitude of the correction signal is adjusted by varying the voltage to the diode attenuator by means of the ten-turn calibrated potentiometer, and has a dynamic range >30 dB.

To operate the MTE the following procedure is suggested:

- (1) Connect the MTE power cord located on the front panel (Figure 4) to 110 Vac, 60 Hz.
- (2) Turn the power switch, located on the attenuator control unit (Figure 12), to ON and allow the MTE to warm up and stabilize for approximately 30 minutes.
- (3) Using a convenient calibrated indicator (spectrum analyzer or chart recorder) obtain a pattern of the distorted signal that is to be corrected.
- (4) Connect the distorted signal to the MTE and compare the pattern to that obtained in step 3. Based on the comparison, adjust the time delay and amplitude controls for minimum distortion and the desired pattern.

A wiring diagram of the attenuator control unit is given in Figure 23 and the typical constant current source circuit for each attenuator is given in Figure 24.

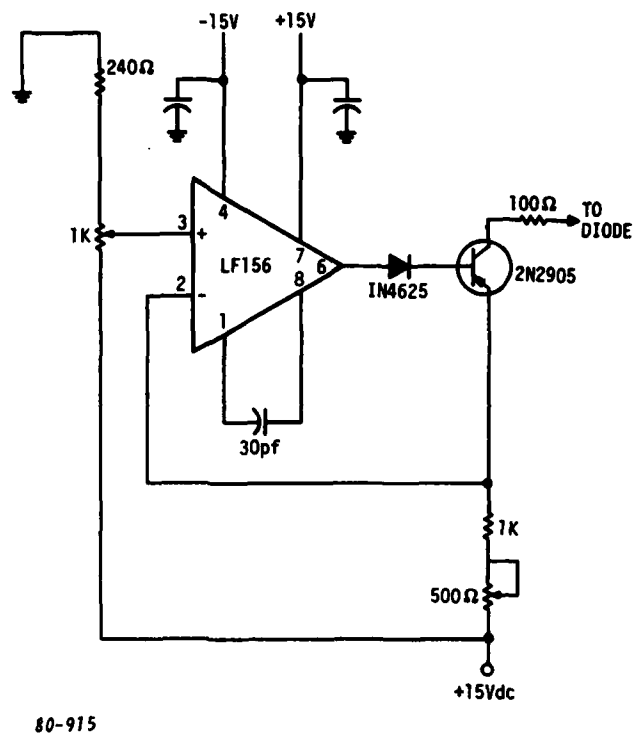


Figure 24. Constant Current Source for Diode Attenuator

6. CONCLUSIONS

A Microwave Transversal Equalizer (MTE) has been successfully designed, fabricated, and tested to determine and evaluate the transfer functions of various microwave components and devices and the capability of reducing time side-lobe distortion in a microwave/radar system. The MTE operates over the 3.0 to 3.5 GHz frequency range and consists of a tapped delay transmission network with a mainline output and 32 coupled outputs spaced at 3.3-ns intervals. Each coupled output or tap has an amplitude control (diode attenuator) and a phase/time delay control (line stretcher). Sixteen taps occur before the mainlobe response and 16 taps occur after the mainlobe response to provide for the equalization of 16 time side lobes before and after the mainlobe. By manually adjusting the amplitude and time delay of the appropriate taps, a time side lobe can be canceled or reduced to a very low level.

Operation of the MTE resulted in successfully reducing a side-lobe level of -8 dB down to -35 dB and side-lobe levels of -18 dB down to -40 dB.

Some areas of further investigation are:

- Complete installation of the required circuitry to utilize all 32 taps contained in the MTE.
- Adapt the MTE for automatic control and interface with computer commands.

7. REFERENCES

- 1. J. J. Taub and G. P. Kurpis, "Microwave Transversal Equalizer," Microwave Journal, 1969.**
- 2. Unitrode Application Note NW-70-1, "General Information on Using Unitrode PIN-Diodes in RF Applications."**
- 3. Unitrode Application Note NW-70-2, "Design Curves for RF Switches Using the UM 4000 Series PIN-Diodes."**